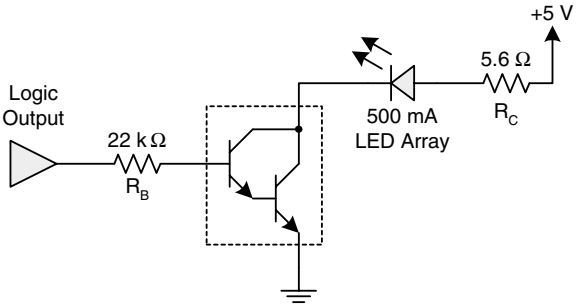

FIGURE 13.16 NPN Darlington pair LED driver.

transistor to the base of the second. As before, the betas multiply, but now V_{BE} is doubled to 1.4 V, because the two base-emitter junctions are in series. The higher V_{BE} reduces the base current from the previous example to roughly 0.06 mA, because the same value of R_B, 22 kΩ, is used. However, with an overall beta of approximately 10,000, the LED array is adequately driven.

13.6 LOGIC FUNCTIONS WITH THE BJT

The preceding circuits are binary amplifiers. In response to a small binary current input, a larger binary output current is generated. Looking at these circuits another way reveals that they are very basic logic gates: inverters. Consider the now familiar circuit in Fig. 13.17a. Rather than driving a high-current load, the output voltage is taken at the collector. When a TTL logic 0 is driven in, R_C pulls the output up to logic 1, 5 V. When a TTL logic 1 is driven in, the transistor saturates and drives the output down to logic 0, $V_{CE\ (SAT)}$. Logic gates in bipolar ICs are more complex than this, but the basic idea is that a simple inverter can be constructed with discrete transistors if the need arises. This discrete inverter can be transformed into a NOR gate by adding a second transistor in parallel with

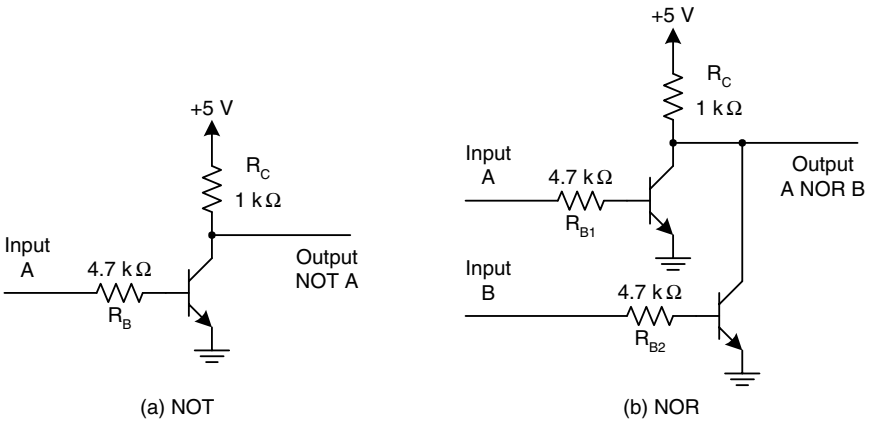

FIGURE 13.17 NPN NOT and NOR gates.

the one already present. In doing so, the output is logic 1 whenever both inputs are logic 0. As soon as one input is driven to logic 1, the accompanying transistor pulls the common V_C output node toward ground and logic 0. An advantage of creating logic gates from discrete transistors is that incompatible voltage domains can be safely bridged. In this example, the logic output is 5 V compatible, while the input can be almost any range of voltages as long as the transistor's specifications are not violated. This voltage conversion function would not be possible over such a wide range with normal bipolar or CMOS logic ICs.

It has been previously mentioned that TTL, or bipolar, logic outputs are asymmetrical in their 0 and 1 logic level drive strengths. A TTL output, shown in Fig. 13.18, consists of a *totem pole* output stage and a driver, or buffer, stage that passes the 0/1 logic function result to the output stage. It is called a totem pole output stage, because the vertical stack of two transistors and a diode somewhat resembles the layering of carvings on a totem pole. Classic TTL logic is composed entirely of NPN transistors, because PNP transistors are more difficult to fabricate on an integrated circuit.

When Q1 is turned on, its emitter voltage, V_{E1}, is fixed at 0.7 V by Q2. Q1 is driven into saturation by the logic circuit (not shown), which brings its collector voltage, V_{C1}, down to $V_{CE\ (SAT)} + V_{E1}$, which is approximately equal to 0.9 V. The saturation voltage of Q1 is approximately 0.2 V, because a sufficient current is injected into the base of Q1. This causes Q2 to saturate as well, driving an output level of $V_{CE\ (SAT)}$, 0.2 V or less. A logic 0 is driven strongly, because there is a direct, low-impedance path to ground through the saturated Q2. Turning our attention up to Q3, the transistor's base-emitter junction would normally be forward biased when $V_{C1} = V_{B3} = 0.9$ V and $V_{E3} = 0.2$ V. The presence of the diode prevents this from happening by increasing the forward-bias threshold by 0.7 V. Therefore, Q3 is in cutoff when Q2 is in saturation.

The resistors surrounding Q1 pull its collector and emitter to the respective voltage rails when Q1 is turned off by the logic circuit. This causes Q2 to turn off and Q3 to turn on by raising V_{B3} to 5 V. When $V_{B3} = 5$ V, $V_{E3} = 4.3$ V, and the output voltage is dropped an additional 0.7 V by the diode to 3.6 V when the load current is small. For small currents, Q3 remains in the active mode, and the output voltage is a function of the drop across the 1.6-kΩ resistor, V_{BE3}, and V_{DIODE}. As the load current increases, Q3 saturates, and the output voltage becomes a function of the drop across the 130 Ω resistor, $V_{CE\ (SAT)}$, and V_D. The impedance from the 5-V supply to the output is greater than for the logic-0 case, which is the reason that TTL logic drives a weaker logic 1.

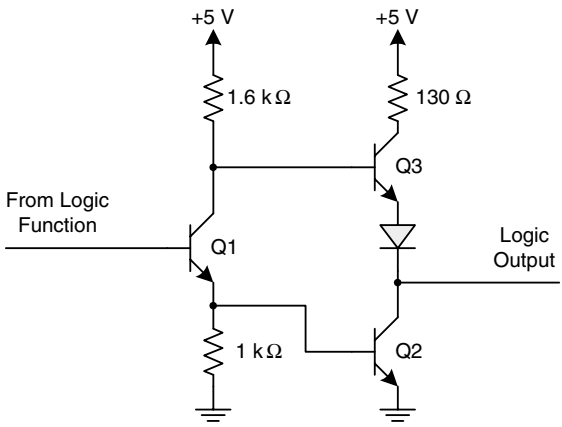

FIGURE 13.18 TTL driver.